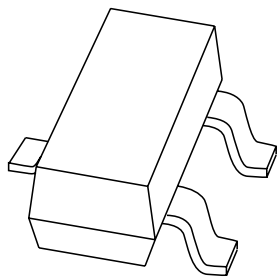


DATA SHEET



PMBT3904 NPN switching transistor

Product specification
Supersedes data of 1999 Apr 27

2004 Jan 12

NPN switching transistor

PMBT3904

FEATURES

- Collector current capability $I_C = 200 \text{ mA}$
- Collector-emitter voltage $V_{CEO} = 40 \text{ V}$.

APPLICATIONS

- General switching and amplification.

DESCRIPTION

NPN switching transistor in a SOT23 plastic package.
PNP complement: PMBT3906.

MARKING

TYPE NUMBER	MARKING CODE ⁽¹⁾
PMBT3904	*1A

Note

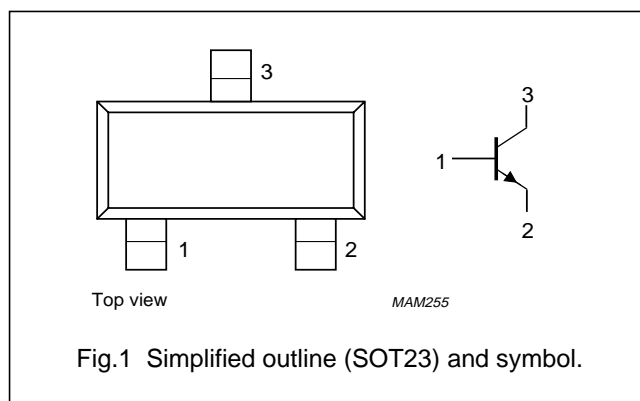
- * = p : Made in Hong Kong.
* = t : Made in Malaysia.
* = W : Made in China.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	40	V
I_C	collector current (DC)	200	mA

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PMBT3904	–	plastic surface mounted package; 3 leads	SOT23

NPN switching transistor

PMBT3904

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	40	V
V_{EBO}	emitter-base voltage	open collector	–	6	V
I_C	collector current (DC)		–	200	mA
I_{CM}	peak collector current		–	200	mA
I_{BM}	peak base current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1	500	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS $T_{amb} = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0$; $V_{CB} = 30\text{ V}$	–	50	nA
I_{EBO}	emitter cut-off current	$I_C = 0$; $V_{EB} = 6\text{ V}$	–	50	nA
h_{FE}	DC current gain	$V_{CE} = 1\text{ V}$; see Fig.2; note 1 $I_C = 0.1\text{ mA}$ $I_C = 1\text{ mA}$ $I_C = 10\text{ mA}$ $I_C = 50\text{ mA}$ $I_C = 100\text{ mA}$	60 80 100 60 30	– – 300 – –	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}$; $I_B = 1\text{ mA}$	–	200	mV
		$I_C = 50\text{ mA}$; $I_B = 5\text{ mA}$	–	300	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = 10\text{ mA}$; $I_B = 1\text{ mA}$	650	850	mV
		$I_C = 50\text{ mA}$; $I_B = 5\text{ mA}$	–	950	mV
C_c	collector capacitance	$I_E = I_e = 0$; $V_{CB} = 5\text{ V}$; $f = 1\text{ MHz}$	–	4	pF
C_e	emitter capacitance	$I_C = I_c = 0$; $V_{BE} = 500\text{ mV}$; $f = 1\text{ MHz}$	–	8	pF

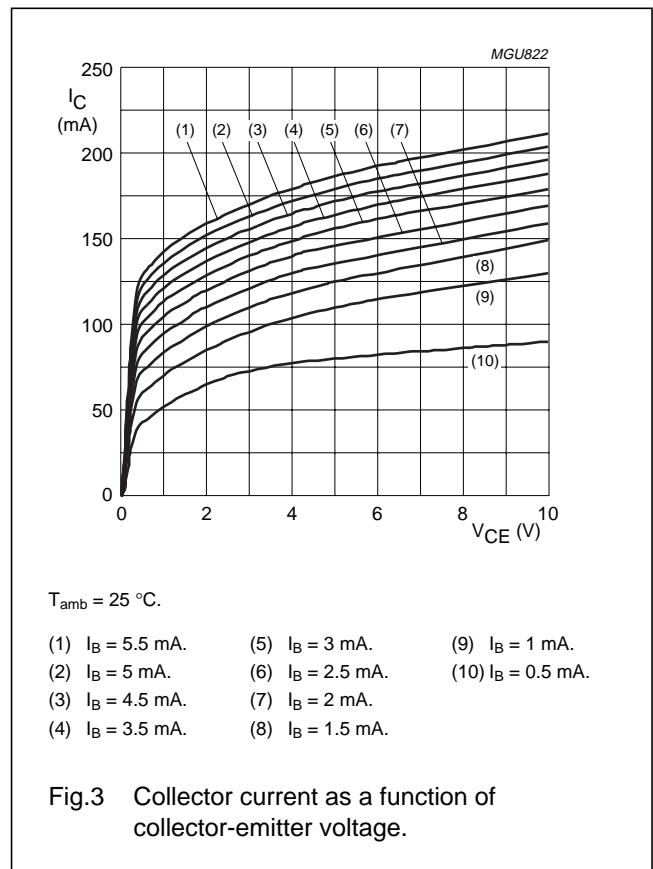
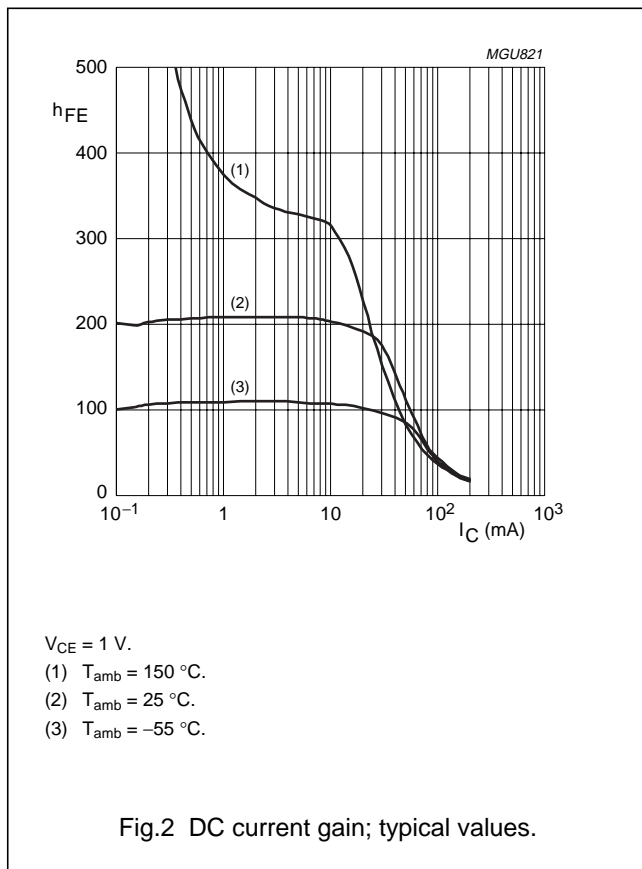
NPN switching transistor

PMBT3904

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_T	transition frequency	$I_C = 10 \text{ mA}; V_{CE} = 20 \text{ V};$ $f = 100 \text{ MHz}$	300	–	MHz
F	noise figure	$I_C = 100 \mu\text{A}; V_{CE} = 5 \text{ V}; R_S = 1 \text{ k}\Omega;$ $f = 10 \text{ Hz to } 15.7 \text{ kHz}$	–	5	dB
Switching times (between 10% and 90% levels); see Fig.3					
t_d	delay time	$I_{Con} = 10 \text{ mA}; I_{Bon} = 1 \text{ mA};$ $I_{Boff} = -1 \text{ mA}$	–	35	ns
t_r	rise time		–	35	ns
t_s	storage time		–	200	ns
t_f	fall time		–	50	ns

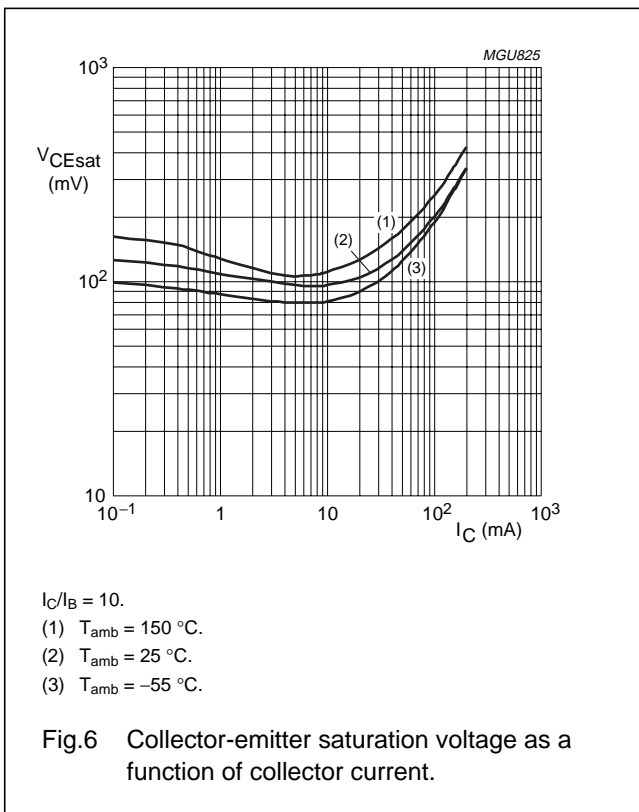
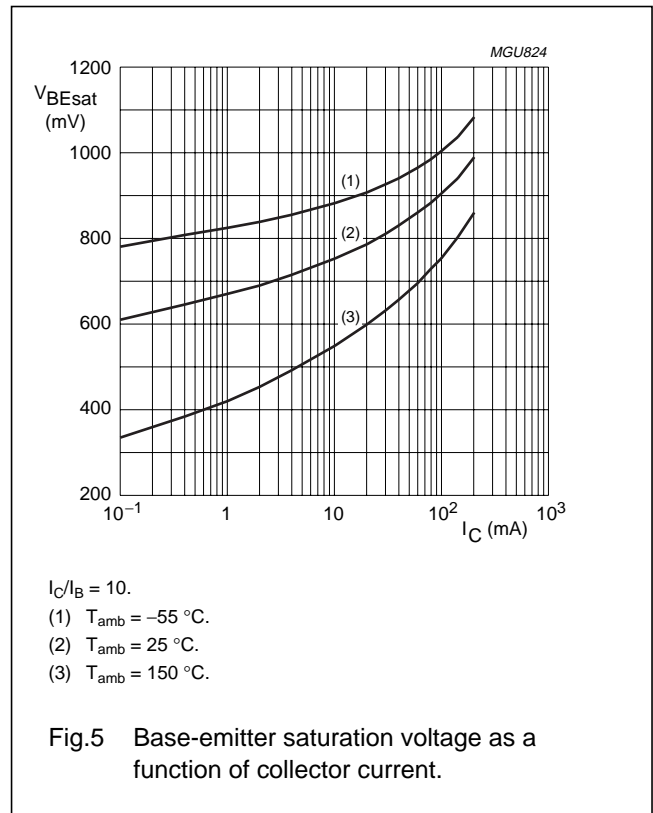
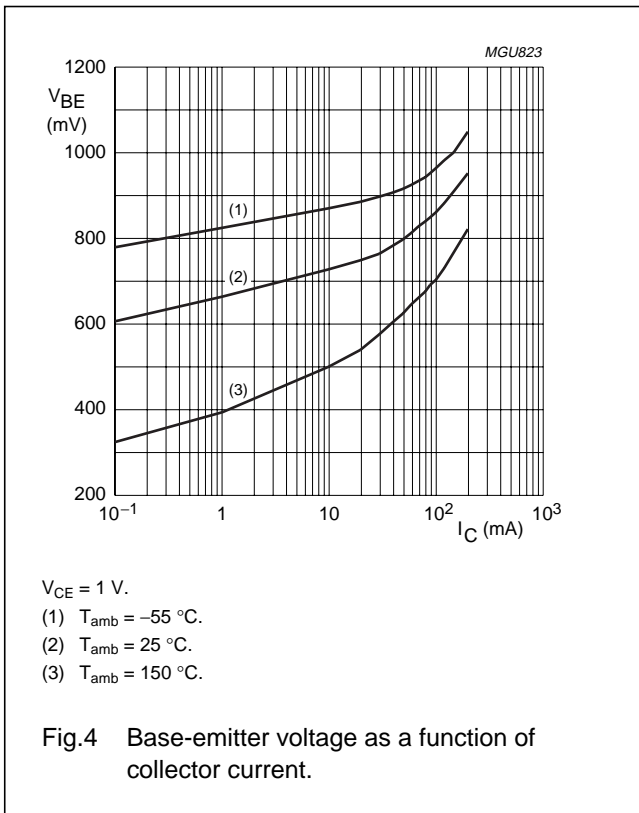
Note

1. Pulse test: $t_p \leq 300 \mu\text{s}; \delta \leq 0.02$.



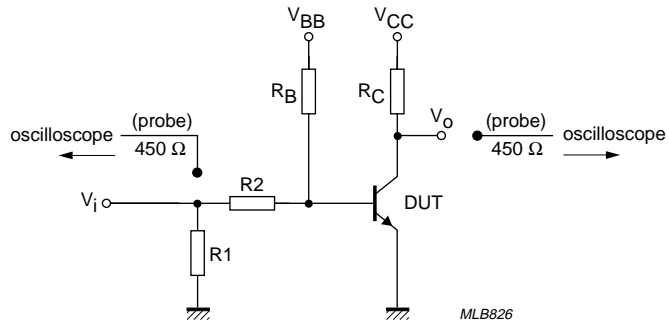
NPN switching transistor

PMBT3904



NPN switching transistor

PMBT3904



$V_i = 5 \text{ V}$; $T = 500 \mu\text{s}$; $t_p = 10 \mu\text{s}$; $t_r = t_f \leq 3 \text{ ns}$.
 $R_1 = 56 \Omega$; $R_2 = 2.5 \text{ k}\Omega$; $R_B = 3.9 \text{ k}\Omega$; $R_C = 270 \Omega$.
 $V_{BB} = -1.9 \text{ V}$; $V_{CC} = 3 \text{ V}$.
 Oscilloscope: input impedance $Z_i = 50 \Omega$.

Fig.7 Test circuit for switching times.

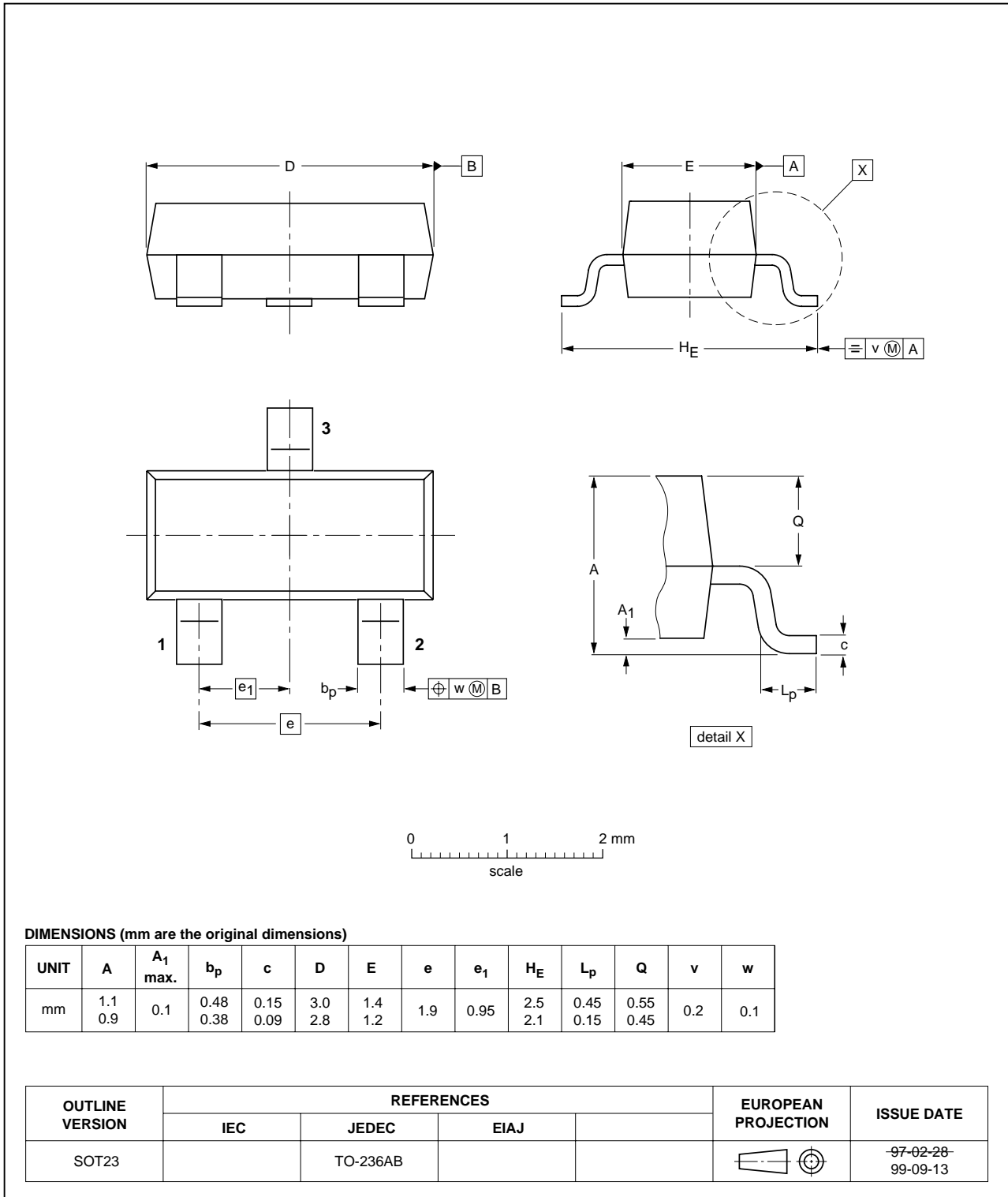
NPN switching transistor

PMBT3904

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT23



NPN switching transistor

PMBT3904

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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